Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

1. (Canceled)

2. (Currently Amended) ~~The~~ A phase comparator circuit ~~as defined in claim 1~~ for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, said phase comparator circuit characterized in that;

said data signal is inputted to a first latch circuit and a second latch circuit, said first latch circuit performs the latching operation thereof with a first clock signal, and said second latching circuit performs the latching operation thereof with the second clock signal, as being an inverted clock signal of said first clock signal;

the output of said first latching circuit is inputted to a third latch circuit, the output of said second latch circuit is inputted to a fourth latch circuit, said third latch circuit performs the latching operation thereof with said second clock signal, and said fourth latch circuit performs the latching operation thereof with said first clock signal;

~~wherein~~ the output of said second latch circuit is connected to a first delay circuit, an exclusive OR of the output from the first delay circuit and the output from said third latch circuit is used as ~~said~~ a first phase error signal; and

the output of said first latch circuit is connected to a second delay circuit, an exclusive OR of the output from said second delay circuit and the output from said fourth latch circuit is used as ~~said~~ a second phase error signal.

3. (Currently Amended) A phase comparator circuit for operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, said phase comparator circuit characterized in that;

a first phase error signal, representing the phase difference between the transition point of said data signal and the rising edge of a first clock signal as the pulse width, is outputted, wherein the pulse width of said first phase error signal is extended by the time width corresponding to the unit time width of said data signal; and

a second phase error signal, representing the phase difference between the transition point of said data signal and the rising edge of a second clock signal as being the inverted clock signal of said first clock signal, is outputted, wherein the pulse width of said second phase error signal is extended by the time width corresponding to the unit time width of said data signal.

4. (Original) The phase comparator circuit as defined in claim 3, wherein, when the transition has occurred between 2 consecutive data in said data signal, a first reference signal, having a time width ranging from the rising edge of said second clock signal to the rising edge of said first clock signal, is outputted in order to determine the increase or the decrease of the pulse width of said first phase error signal; and

when the transition has occurred between 2 consecutive data in said data signal, a second reference signal, having a time width ranging from the rising edge of said first clock signal to the rising edge of said second clock signal, is outputted in order to determine the increase or decrease of the pulse width of said second phase error signal.

5. (Canceled)

6. (Canceled)

7. (Currently Amended) A CDR circuit including a phase comparator circuit, a charge pump circuit and a loop filter, operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, and characterized in that;

said phase comparator circuit outputs a first phase error signal, representing the pulse width as being the phase difference between the transition point of the said data signal and the rising edge of said clock signal, the pulse width of said first phase error signal being extended by the time width corresponding to the unit time width of said data signal, and a second phase error signal, representing the pulse width as being the phase difference between the transition point of said data signal and the falling edge of said clock signal, the pulse width of said second phase error signal being extended by the time width corresponding to the unit time width of said data signal;

when the transition has occurred between two consecutive data in said data signal, said phase comparator circuit outputs a first reference signal, having a time width ranging from the falling edge of said clock signal to the rising edge of said clock signal, and a second reference signal, having a time width ranging from the rising edge of said clock signal to the falling edge of said clock signal;

said charge pump circuit comprises a first charge pump circuit for receiving the input of said first phase error signal and the input of said reference signal, and a second

charge pump circuit for receiving the input of said second phase error signal and said second reference signal; and

the source current to flow into said loop filter according to the said first and second phase error signals and the sink current to flow into said loop filter according to said first and second reference signals are designed to become equal with each other when the phase of said data signal and the phase of said clock signal coincide with each other.

8. (Original) The CDR circuit as defined in claim 7, wherein said charge pump circuit includes a current supply means to be controlled by external voltage so as to adjust the ratio between said source current and said sink current.

9. (Canceled)

10. (Amended) A CDR circuit including a phase comparator circuit, a charge pump circuit and a loop filter, operating with a clock signal whose period is 2 times the unit time width of an inputted data signal, and <u>said phase comparator circuit</u> characterized in that;

<u>said data signal is inputted to a first latch circuit and a second latch circuit, said first latch circuit performs the latching operation thereof with a first clock signal, and said second latching circuit performs the latching operation thereof with the second clock signal, as being an inverted clock signal of said first clock signal;</u>

<u>the output of said first latching circuit is inputted to a third latch circuit, the output of said second latch circuit is inputted to a fourth latch circuit, said third latch circuit performs</u>

the latching operation thereof with said second clock signal, and said fourth latch circuit performs the latching operation thereof with said first clock signal;

the output of said second latch circuit is connected to a first delay circuit, an exclusive OR of the output from the first delay circuit and the output from said third latch circuit is used as first phase error signal;

the output of said first latch circuit is connected to a second delay circuit, an exclusive OR of the output from said second delay circuit and the output from said fourth latch circuit is used as a second phase error signal; and

~~said phase comparator circuit extends the pulse width of the phase error signal, as being the phase difference between the transition point of said data signal and the transition point of said clock signal, to any desired amount and outputs the~~ said first and second phase error signal are outputted to said charge pump circuit.

11. (Canceled)

12. (Canceled)